

WHAT IS CLAIMED IS:

1                   1.     A system timer for controlling the timing at which a  
2 communication device communicates, said system timer comprising:  
3                   a memory device adapted to store a set of software instructions;  
4                   a processor coupled to said memory device, said processor being  
5 adapted to execute any of said software instructions in any of a plurality of  
6 sequences, each of said sequences causing said processor to generate a  
7 corresponding set of control signals, each of said corresponding set of control  
8 signals being adapted to enable communication by said communication device  
9 in one of a multiplicity of communication formats, wherein each of said  
10 communication formats defines the timing at which a set of data is  
11 communicated by said communication device.

1                   2.     The system timer of claim 1 wherein said processor  
2 comprises a first processor and further wherein said communication device  
3 comprises a second processor, wherein said plurality of sequences in which  
4 said first processor executes said software instructions is controlled by said  
5 second processor.

1                   3.     The system timer of claim 2 wherein said system timer  
2 further comprises a memory register for storing addresses, said addresses  
3 indicating a set of locations at which at least some of said software instructions  
4 are stored in said memory device, wherein said first processor is adapted to  
5 extract said addresses from said memory register and to execute said software  
6 instructions located at said addresses thereby causing said first processor to  
7 execute said software instructions in a sequence defined by an order in which  
8 said addresses are stored in said memory register.

1           4.     The system timer of claim 3 wherein said second  
2 processor controls said plurality of sequences in which said first processor  
3 executes said software instructions by controlling said order in which said  
4 addresses are stored in said memory register.

1           5.     The system timer of claim 4 wherein said software  
2 instructions comprise a first software instruction that, when executed by said  
3 first processor, causes said first processor to extract one of said addresses  
4 stored in said memory register and to execute a second software instruction  
5 located at said one of said addresses provided that said second processor has  
6 caused at least one of said addresses to be stored in said memory register.

1           6.     The system timer of claim 5 wherein said first software  
2 instruction further causes said first processor to execute a third software  
3 instruction stored in said memory device provided that said second processor  
4 has not stored said at least one address in said memory register, wherein an  
5 address at which said third software instruction is stored in said memory device  
6 is specified in said first software instruction.

1           7.     The system timer of claim 2 wherein said set of software  
2 instructions stored in said memory device comprises a first instruction, said  
3 first instruction, when executed by said first processor, causing said first  
4 processor to execute a first sequence of software instructions provided that a  
5 condition has been satisfied by said second processor and further causing said  
6 first processor to execute a second sequence of software instructions provided  
7 that said condition has not been satisfied.

1                   8.     The system timer of claim 7 wherein said first sequence of  
2 software instructions begins with a second instruction located at an address  
3 specified in said first instruction.

1                   9.     The system timer of claim 7 wherein said condition  
2 comprises a mode bit being set to a first logic level.

1                   10.    The system timer of claim 7 wherein said condition  
2 comprises an equation being equal to a predefined value.

1                   11.    The system timer of claim 10 wherein said equation being  
2 equal to said predefined value depends upon whether a set of mode bits have  
3 been set by said second processor.

1                   12.    The system timer of claim 2 wherein said plurality of  
2 sequences comprises a first sequence that causes said communication device to  
3 perform single slot communication and wherein said second processor is  
4 adapted to modify said first sequence to a second sequence that causes said  
5 communication device to perform multi-slot communication.

1                   13.    The system timer of claim 2 wherein said second  
2 processor controls said sequence by setting a control bit stored in a memory  
3 register.

1                   14.    The system timer of claim 2 wherein said second  
2 processor comprises a digital signal processor.

1                   15.    The system timer of claim 2 wherein said second  
2 processor comprises a microprocessor.

1           16. The system timer of claim 1 wherein said plurality of  
2 sequences comprises a first sequence of said software instructions that, when  
3 executed by said first processor, enables operation of said communication  
4 device in a first mode, wherein said plurality of sequences further comprises a  
5 second sequence of said software instructions that, when executed by said first  
6 processor, enables operation of said communication device in a second mode,  
7 and wherein said second processor is adapted to cause said first processor to  
8 switch between executing said first and second sequences thereby causing said  
9 communication device to switch between said first and second modes.

1           17. The system timer of claim 16 wherein said first mode  
2 comprises a stand by mode and wherein said second mode comprises an  
3 acquisition mode.

1           18. The system timer of claim 16 wherein said first mode  
2 comprises an acquisition mode and wherein said second mode comprises a  
3 steady state mode.

1           19. The system timer of claim 1 wherein said multiplicity of  
2 communication formats comprises a single slot communication format.

1           20. The system timer of claim 1 wherein said multiplicity of  
2 communication formats comprises a multi-slot communication format.

1           21. A system timer for controlling a timing at which a set of  
2 data frames are communicated between a first communication device and a  
3 second communication device, wherein said system timer is disposed in said  
4 first communication device, said system timer comprising:

5           a processor adapted to adjust a frame length during which a first

6 frame of data is communicated, wherein adjusting said frame length of said  
7 first frame of data causes a start time of a second frame of data to be adjusted  
8 and further wherein adjusting said start time of said second frame of data  
9 causes a communication time slot to be adjusted, said communication time slot  
10 occurring at a fixed start time relative to said start time of said second frame of  
11 data.

1 22. The system timer of claim 21 wherein said frame length  
2 comprises a first frame length, said system timer further comprising:

3 a counter adapted to count at a rate that corresponds to a set of  
4 clock pulses and further being adapted to wrap to zero upon reaching said first  
5 frame length;

6 a first memory register for storing said first frame length;

7 a second memory register for storing a second frame length;

8 said processor being adapted to adjust said first frame length by  
9 causing said counter to wrap to zero upon reaching said second frame length.

1 23. The system timer of claim 22 wherein said communication  
2 time slot comprises a first communication time slot and further wherein said  
3 processor is further adapted to adjust said counter by an amount of time equal  
4 to an offset value upon executing a software instruction thereby causing a time  
5 at which a second communication time slot occurs to be adjusted by said  
6 amount of time equal to said offset value.

1 24. The system timer of claim 23 wherein said software  
2 instruction includes a field for containing data that indicates whether said  
3 counter will be incremented by said offset value.



11 time slot after said first time slot has ended.

1 30. The system timer of claim 29 wherein said first time slot is  
2 fixed relative to a frame start and wherein said processor is adapted to adjust  
3 said first time slot in said first direction by adjusting said frame start in said  
4 first direction.

1 31. The system timer of claim 30 wherein said frame start is  
2 associated with a first frame and wherein said processor is adapted to adjust  
3 said frame start in said first direction by adjusting a frame length of a second  
4 frame, said second frame preceding said first frame.

1 32. The system timer of claim 31 further comprising a  
2 memory register for storing a frame length value and a counter associated with  
3 said timing at which said frames are communicated, said counter being adapted  
4 to wrap to zero upon reaching said frame length value, wherein said processor  
5 is adapted to adjust said frame length of said second frame by changing said  
6 frame length value during said second frame.

1 33. The system timer of claim 29 further comprising a counter  
2 associated with said timing at which said frames are communicated, wherein  
3 said processor adjusts said second time slot in said second direction by causing  
4 said counter to be adjusted.

1 34. The system timer of claim 29 wherein adjusting said first  
2 time slot in said first direction causes said first time slot to occur later and  
3 wherein said step of adjusting said second time slot in said second direction  
4 causes said second time slot to occur earlier.

1           35. The system timer of claim 34 wherein said first time slot  
2 comprises a receive slot during which said first communication device is  
3 configured to receive data from said second communication device and  
4 wherein said second time slot comprises a transmit slot during which said first  
5 communication device is configured to transmit data to said second  
6 communication device.

1           36. The system timer of claim 34 wherein said receive slot is  
2 adjusted to occur later so that said data transmitted by said second  
3 communication device has sufficient time to reach said first communication  
4 device and wherein said transmit slot is adjusted to occur earlier so that said  
5 data transmitted by said first communication device has sufficient time to reach  
6 said second communication device.

1           37. A method for controlling the timing at which a  
2 communication device communicates, said communication device comprising  
3 a first processor and a system timer, said system timer comprising a second  
4 processor and a memory device adapted to store a set of software instructions,  
5 said method comprising the steps of:

6           causing said second processor to execute a set of software  
7 instructions in any of a plurality of sequences, each of said sequences causing  
8 said second processor to generate a corresponding set of control signals, each  
9 of said corresponding set of control signals being adapted to enable  
10 communication by said communication device in one of a multiplicity of  
11 communication formats, wherein each of said communication formats defines  
12 the timing at which a set of data is communicated by said communication  
13 device; and,

14           causing said first processor to define said sequences in which said  
15 second processor executes said software instructions.



1           38. The method of claim 37 wherein a first of said sequences  
2 causes said communication device to communicate in a first timing format and  
3 wherein a second of said sequences causes said communication device to  
4 communicate in a second timing format.

1           39. The method of claim 37 wherein said first timing format  
2 comprises a single slot timing format and wherein said second timing format  
3 comprises a multi-slot timing format.

1           40. The method of claim 37 wherein a first of said sequences  
2 defined by said first processor causes said communication device to operate in  
3 a first mode and wherein a second of said sequences defined by said first  
4 processor causes said communication device to communicate in a second  
5 mode.

1           41. The method of claim 39 wherein said first mode comprises  
2 a stand by mode and wherein said second mode comprises an acquisition mode.

1           42. The method of claim 40 wherein said first mode comprises  
2 an acquisition mode and wherein said second mode comprises a steady state  
3 mode.

1           43. The method of claim 36 wherein said first processor  
2 defines said sequences in which said second processor executes said software  
3 instructions by storing a set of addresses in an order in a memory register  
4 disposed in said system timer, said set of addresses indicating a set of locations  
5 at which at least some of said software instructions are stored in said memory  
6 device, wherein said second processor is adapted to extract and execute said  
7 addresses from said memory register in said order in which said addresses are  
8 stored.

1           44. The method of claim 36 wherein an order in which said  
2 instructions are executed in at least one of said sequences is dependent upon  
3 said first processor setting a mode bit to a first logic level.

1           45. A method for compensating for a first timing offset  
2 associated with a first time slot and for compensating for a second timing offset  
3 associated with a second time slot, said first time slot and said second time slot  
4 occurring in each of a set of frames, wherein said first time slot occurs before  
5 said second time slot, said method comprising the steps of:  
6           adjusting said first time slot in a first direction during a first  
7 frame, said first time slot being fixed relative to a frame start associated with  
8 said first frame, wherein said first time slot is adjusted in said first direction by  
9 adjusting said frame start associated with said first frame in said first direction;  
10 and,  
11           adjusting said second time slot in a second direction after said  
12 first time slot has ended.

1           46. The method claim 45 wherein said step of adjusting said  
2 first time slot in a first direction during a first frame is performed by adjusting a  
3 frame length associated with a second frame, said second frame preceding said  
4 first frame.

1           47. The method of claim 46 wherein said step of adjusting  
2 said frame length associated with said second frame is performed by changing  
3 a value at which a counter wraps to zero during said second frame.

1           48. The method of claim 45 wherein said step of adjusting  
2 said second time slot in a second direction after said first time slot has ended is  
3 performed by causing a counter to be adjusted.

1                   49. The method of claim 45 wherein said step of adjusting  
2 said first time slot in said first direction causes said first time slot to occur later  
3 and wherein said step of adjusting said second time slot in said second  
4 direction causes said second time slot to occur earlier.

1                   50. The method of claim 44 wherein said first time slot  
2 comprises a receive slot during which a first communication device is  
3 configured to receive a first set of data from a second communication device  
4 and wherein said second time slot comprises a transmit slot during which said  
5 first communication device is configured to transmit a second set of data to  
6 said second communication device.

1                   51. The method of claim 49 wherein said first time slot is  
2 adjusted to occur later so that said first set of data has sufficient time to reach  
3 said first communication device

1                   52. The method of claim 49 wherein said second time slot is  
2 adjusted to occur earlier so that said second set of data has sufficient time to  
3 reach said second communication device.